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Title: LIQUID CRYSTAL DISPLAY DEVICE. ;

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ABSTRACT:

A thin film transistor structure for a liquid crystal display device of the active matrix type wherein leak current is suppressed to stabilize the threshold voltage and the dispersion in gate capacitance coupling and the channel length are minimized is disclosed. The liquid crystal display device comprises a substrate having picture element electrodes arranged in a matrix and switching elements for driving the picture element electrodes, another substrate having opposing electrodes thereon and opposed to the former substrate, and a liquid crystal layer held between the substrates. Each switching element has a multi-gate structure wherein two thin film transistors are connected in series and gate electrodes are electrically connected to each other. Each thin film transistor has a lightly doped drain structure wherein a low density impurity region of the same conductivity type as that of a source region or a drain region is provided at least between the source or drain region and a channel region. At least one of a plurality of such low density impurity regions may have a length or a density different from that of the other low density impurity regions so as to assure sufficient on-current while suppressing the leak current.

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(54) Liquid crystal display device.

(57) A thin film transistor structure for a liquid crystal display device of the active matrix type wherein leak current is suppressed to stabilize the threshold voltage and the dispersion in gate capacitance coupling and the channel length are minimized is disclosed. The liquid crystal display device comprises a substrate (1) having picture element electrodes arranged in a matrix and switching elements for driving the picture element electrodes, another substrate having opposing electrodes thereon and opposed to the former substrate, and a liquid crystal layer held between the substrates. Each switching element has a multi-gate structure wherein two thin film transistors are connected in series and gate electrodes (9) are electrically connected to each other. Each thin film transistor has a lightly doped drain structure (4,5) wherein a low density impurity region (6) of the same conductivity type as that of a source region (3,4) or a drain region is provided at least between the source or drain region and a channel region (2). At least one of a plurality of such low density impurity regions may have a length or a density different from that of the other low density impurity regions so as to assure sufficient on-current while suppressing the leak current.

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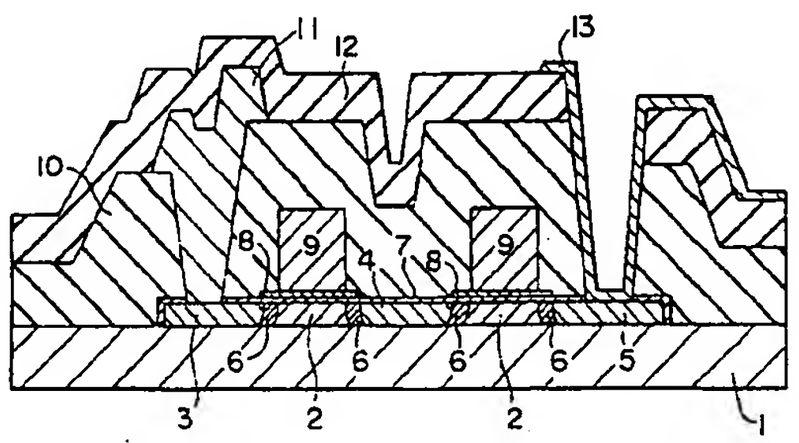

EP 0 589 478 A3